

**In the Claims:**

Please amend the claims as indicated below.

1. (Currently Amended) A power semiconductor device, comprising:  
an output transistor having  
main cells and sense cells,  
a control input connected to the main and sense cells, and  
main and sense cell controlled outputs;  
an output terminal connected to one of the main cell controlled outputs for  
connection to a load;  
a feedback circuit for measuring the voltage across the main cell controlled  
outputs of the output transistor and for controlling the voltage on the control input, the  
feedback circuit including a first comparator configured to output a signal responsive to  
increase the voltage across the main cell controlled outputs if the magnitude of the  
voltage across the main cell controlled outputs falls below a predetermined value and a  
diode connected in series between the output of the first comparator and the control input,  
the diode orientated to pass current between the output of the first comparator and the  
control input to increase the voltage across the main cell controlled outputs;  
a reference current supply feeding a reference current through the sense cell  
controlled outputs; and  
a second comparator arranged to compare the voltages across the main cell  
controlled outputs and the sense cell outputs and to output a low-current signal when the  
magnitude of the voltage across the main cell controlled outputs falls below that across  
the sense cell outputs.
2. (Currently Amended) A power semiconductor device according to claim 1  
wherein the feedback circuit further includes a voltage reference, and the first [[a]]  
comparator is connected across the main cell outputs for comparing the voltage across the  
main cell outputs with the voltage reference, the output of the first comparator ~~of the~~  
~~feedback circuit being connected through the~~ [[a]] diode to the control input, the diode  
being forward biased ~~orientated~~ to pass current between the output of the first comparator

and the control input to change the control voltage in a direction to increase the on-resistance of the main cells responsive to when the voltage across the main cell outputs falling falls below the voltage reference predetermined value and the diode being reverse biased responsive to the voltage across the main cell outputs being above the voltage reference.

3. (Previously Presented) A power semiconductor transistor according to claim 1 wherein the main and sense cells are FET main and sense cells and the gates of the FETs are connected in common to the control input and the sources and drains of the FETs of the main and sense cells form the outputs of the FETs.

4. (Previously presented) A power semiconductor device according to claim 3, in the form of a high side device wherein:

the drains of the sense and main cells are connected in common to a battery terminal;

the source of the main cells is connected to the output terminal; and

the source of the sense cells is connected to the reference current supply, the reference current supply being a reference current sink.

5. (Previously presented) A power semiconductor circuit including a power semiconductor device according to claim 1 further comprising a load connected to the output terminal.

6. (Currently Amended) A method of operating a semiconductor device, the device including an output transistor circuit having main cells and sense cells, a control input connected to the main and sense cells, and main and sense cell controlled outputs, the method comprising:

driving the main and the sense cells in common;

driving a load from one of the main cell controlled outputs feeding a reference current through the sense cell controlled outputs;

measuring the voltage across the main cell controlled outputs and controlling the voltage on the control input to increase the voltage across the main cell controlled outputs responsive to if the magnitude of the voltage across the main cell controlled outputs falling falls-below a predetermined value;

outputting a signal using a comparator responsive to the magnitude of the voltage across the main cell controlled outputs;

passing current between the output of the comparator and the control input to increase the voltage across the main cell controlled out, the current being passed through a diode that is connected in series between the output of the comparator and the control input; and

comparing the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs.

7. (Currently Amended) A method according to claim 6 wherein the step of measuring the voltage across the main cell controlled outputs includes ~~is performed by:~~

comparing the voltage across the main cell controlled outputs with a reference voltage using ~~[[a]]~~ the comparator ~~comparators~~;

outputting the signal by the comparator when the magnitude of the voltage across the main cell controlled outputs falls below the reference voltage; and

responsive to the voltage across the main cell controlled outputs, driving the diode being forward biased to pass current between the output of the comparator and the control input from the output of the comparator through a diode the diode being orientated to pass current to change the control input voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the reference voltage predetermined and the diode being reverse biased when the voltage across the main cell outputs is above the reference voltage.

8. (Currently Amended) A device comprising:

an output transistor circuit having main cells and sense cells;

a control input connected to the main and sense cells;  
main and sense cell controlled outputs;  
a first circuit configured and arranged to drive the main and the sense cells in common;  
a second circuit configured and arranged to drive a load from one of the main cell controlled outputs feeding a reference current through the sense cell controlled outputs;  
a measurement circuit configured and arranged to measure the voltage across the main cell controlled outputs and ~~to control~~ controlling the voltage on the control input, the measurement circuit including a comparator configured to output a signal responsive to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the main cell controlled outputs falls below a predetermined value and a diode connected in series between the output of the comparator and the control input, the diode orientated to pass current between the output of the comparator and the control input to increase the voltage across the main cell controlled outputs; and  
a comparison circuit configured and arranged to compare the voltages across the main cell controlled outputs and the sense cell controlled outputs and ~~to output~~ outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs.

9. (Currently Amended) A device according to claim 8, wherein the diode is forward biased to pass current between the output of the comparator and the control input responsive to the voltage across the main cell outputs falling below a predetermined value and the diode is reverse biased responsive to the voltage across the main cell outputs being above the predetermined value ~~comparison circuit is further configured and arranged to output the low-current signal for current driving the control input that is connected to the main and sense cells.~~

10. (Currently Amended) A device according to claim 9, wherein each of the main and sense cells includes a FET-based circuit with a gate terminal, and the measurement ~~comparison~~ circuit is further configured and arranged to drive the control input by outputting the low-current signal.

11. (Previously presented) A device according to claim 9, wherein each of the main and sense cells includes a FET-based circuit with a gate terminal, and wherein the control input is commonly connected to each gate terminal of the main and sense cells for driving the main and sense cells.

12. (Previously presented) A device according to claim 8, further including a load connected between an output terminal of the output transistor and ground.

13. (Currently Amended) A device according to claim 8, further including a battery arranged for providing a voltage reference to the measurement circuit, and for providing power to the main and sense cells.

14. (Currently Amended) A device according to claim 8, further including a battery arranged for providing a voltage reference to the measurement circuit and for providing power to the main and sense cells, and further including a load connected between an output terminal of the output transistor and ground.